Design Concepts For A
588 Channel Data Acquisition & Control System

Kenneth H. Bosin, Spectral Dynamics Inc.

This paper discusses the design methods used to create a data acquisition and control system that is capable of acquiring up to 588 simultaneous channels of synchronously sampled data. This system is operational in world-class facilities throughout the world, including locations in the USA, Brazil, Canada, China, France, Germany, Italy, Japan, UK and others.

Both hardware and software design concepts are presented. A key attribute is the use of scalable and distributed architectures that allows extending the hardware and software features of a base system as laboratory requirements and resources change.

An overview of the supported turn-key applications is also presented. These applications are in the following general categories:

- Single Exciter Control
- Multiple Exciter Control
- Environmental Lab Signal Analysis
- Third-Party Applications

The same system can be used for all of these applications without reconfiguring any hardware or software and without any compromises in performance. Figure 1 provides a simplified block diagram for the system.

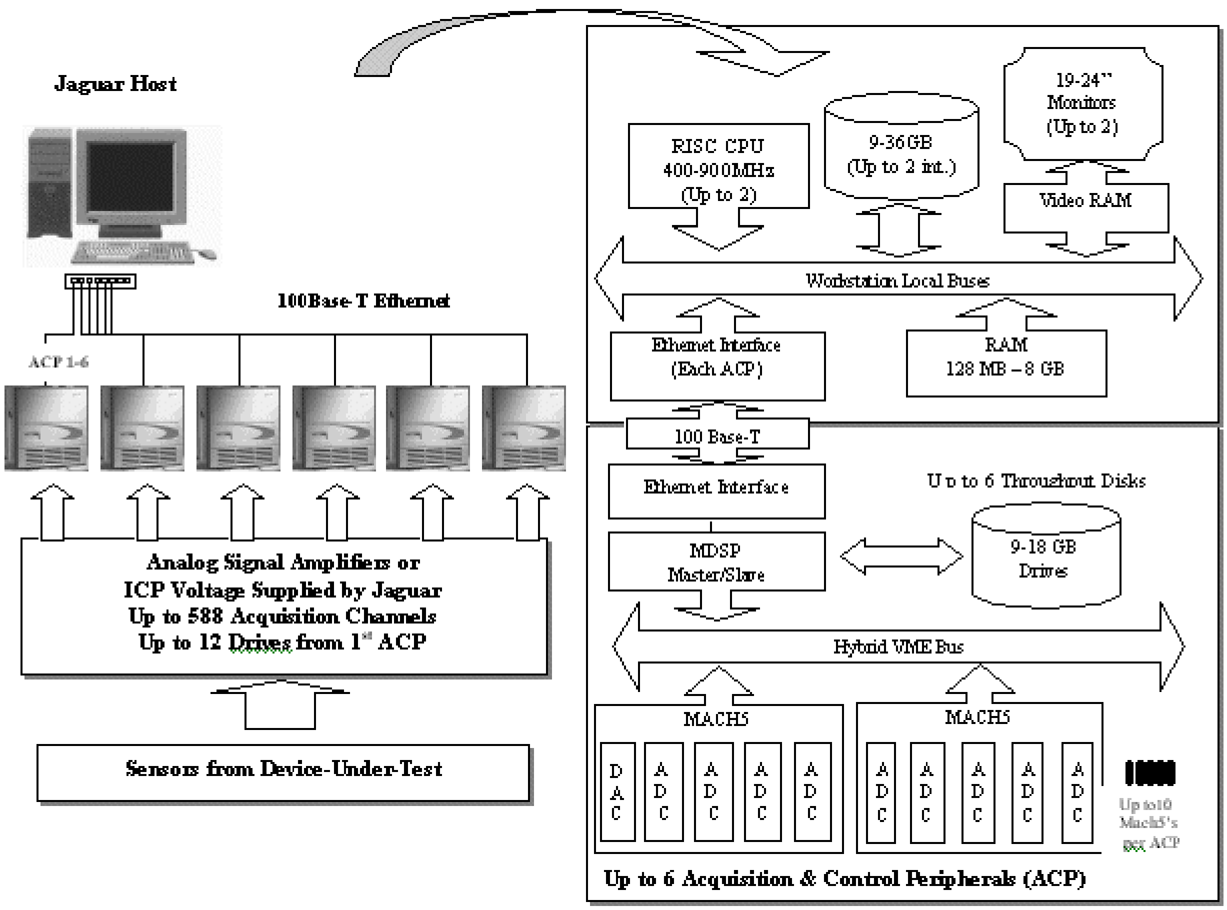

Figure 1. JAGUAR System Block Diagram

System Overview

The acquisition and control peripheral (ACP) houses the input/output channel hardware, DSP hardware, RISC processor and hardware for various interfaces. The ACP is configurable into two chassis sizes that support up to 38 and 98 acquisition channels. Multiple ACPs may be configured to reach the current practical limit of 588 acquisition channels.

The ACP or multiple ACPs are interfaced to a family of commercially available workstations for graphical user interface, host data storage, networking, word processing and other general-purpose applications.

The software architecture is similar for all applications. An overview of the software and hardware design for a system configured with 6 ACPs is shown in Figure 2.

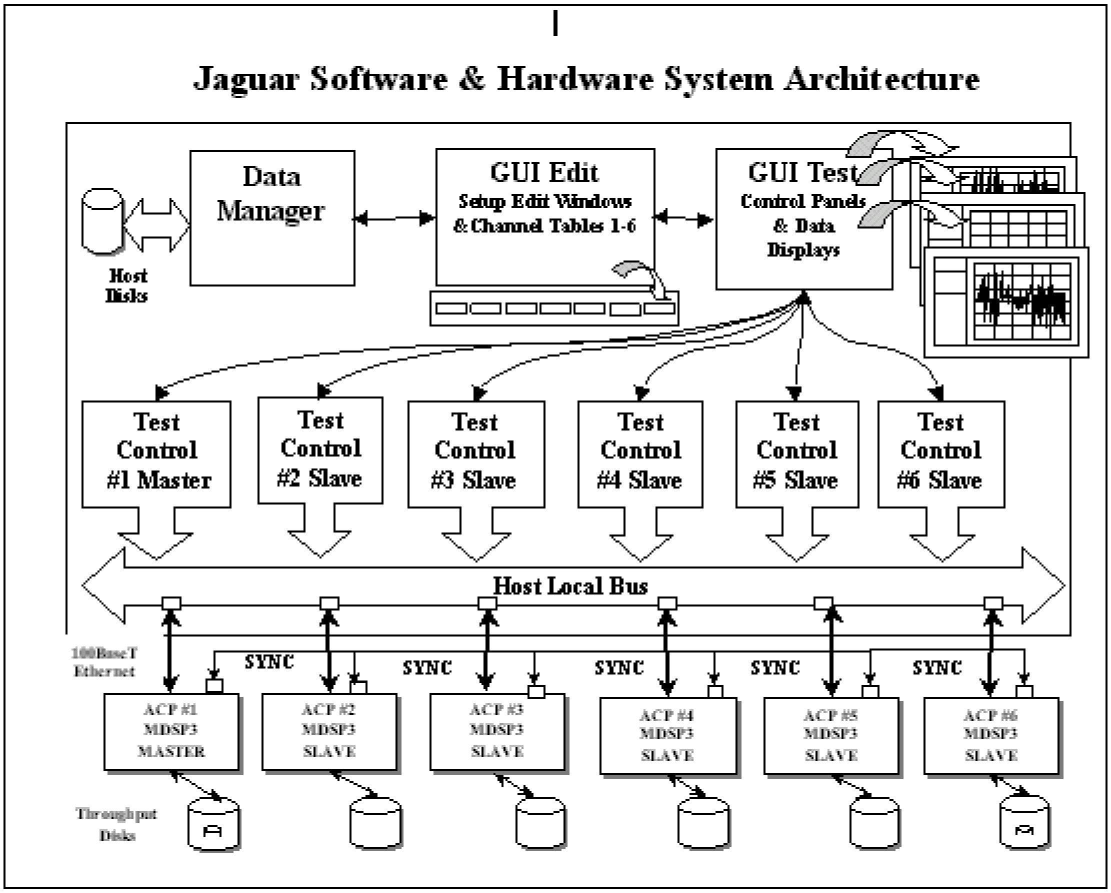

Figure 2. JAGUAR Software & Hardware Architectural Overview

Hardware Design Concepts

The hardware design is distributed and scalable. The basic hardware unit in this architecture is the Acquisition & Control Peripheral (ACP) that is interfaced to a host workstation. The ACP may contain a maximum of either 38 or 98 input channels depending on the size of the selected chassis. Up to 6 ACPs may be synchronized (down to the A-D converter sample) to support the practical limit of up to 588 synchronized input channels. The maximum number of available input channels is also dependent on the number of drive (output) channels installed in the ACP.

The modules and options available for the ACP include:

- Mdsp3 RISC Processor
- Mach5 I/O Channel Boards
- Throughput Disk (TPD) Controller and Drives.

The Mdsp3 RISC processor is the 3rd generation of micro digital signal processors (Mdsp3) used in Spectral Dynamics' products. This processor is available in several CPU speeds and memory sizes. The current models are supplied from a family of processors manufactured by Motorola Computer Products. These designs are based on the highly pipelined family of PowerPC RISC CPUs. The VxWorks Tornado real-time operating system (RTOS) is utilized for its proven critical mission processing.

The Mach5 I/O board supports up to 10 input channels via 5 DSP nodes. Each of the nodes can support 2 input channels with separate A-D converters per channel. Three of the nodes on each Mach5 board can support a Drive-Utility channel pair in place of the Input channel pair. The input and output sections of the board are implemented as daughter cards so that the Mach5 boards may be easily configured. This also allows for increased economies in the manufacturing process and passed-on savings to customers.

The Drive channel includes a 16 bit D-A converter, appropriate smoothing filters, a 48 bit attenuator, offset compensation circuitry and suitable memory for supporting multiple exciter matrix operations. The Utility connector provides access to the unattenuated Drive (COLA) signal typically used in Swept Sine Analysis applications. Figure 3 shows a block diagram for the Output daughter card.

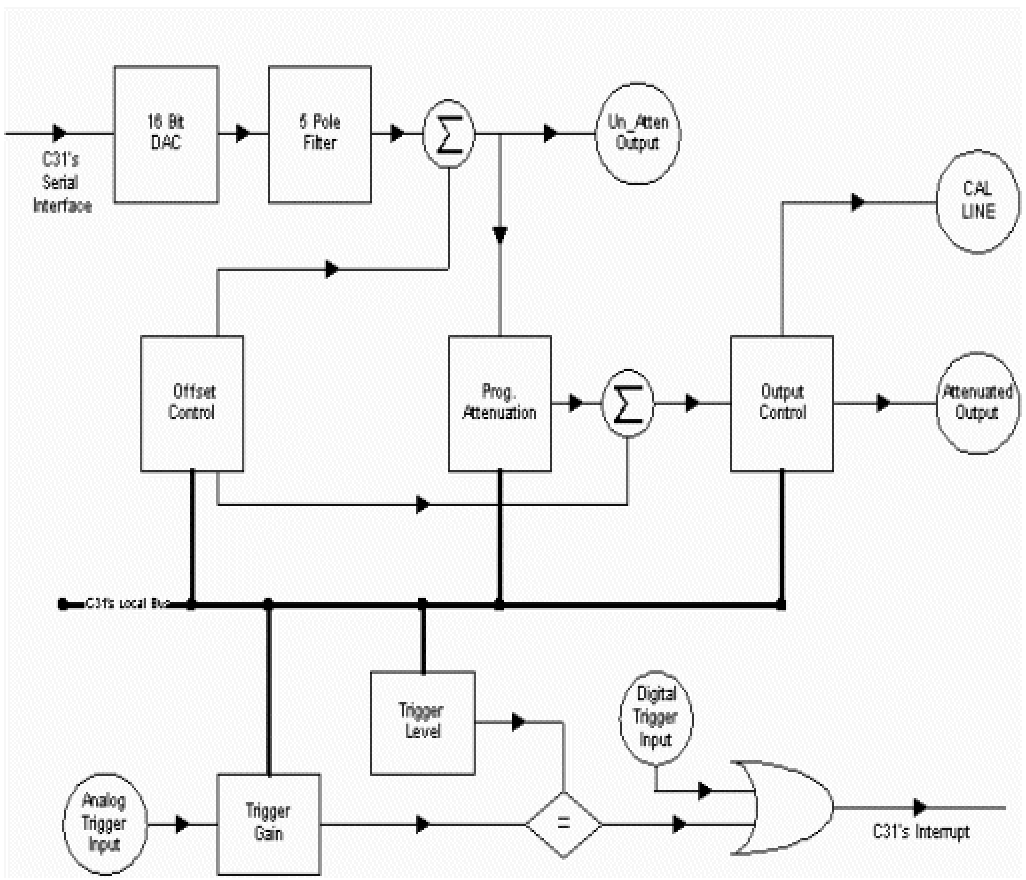

Figure 3. JAGUAR Output Daughter Card

The block diagram for the input daughter card is shown in Figure 4. The design includes the following major sections:

- Input Coupling (AC, DC, ICP 24V not shown).

- Instrumentation amplifier for implementing full-scale auto-ranging in 1dB steps.
- Analog anti-alias filtering.
- 16 bit Sigma-Delta ADC.
- Offset nulling circuitry.
- Computer controlled calibration.

The DSP chips on each node of the digital section of the Mach5 boards provide for additional input and output processing. Digital filtering and decimation is provided for most applications so that only the data of interest is processed.

The micro-code for the DSP chips is downloaded at run-time for each application. Different code may be loaded into various DSPs within an application depending on the type of processing requested for the various channels. For the Swept Sine applications, individual digital tracking filters are implemented via download into each of the active channels.

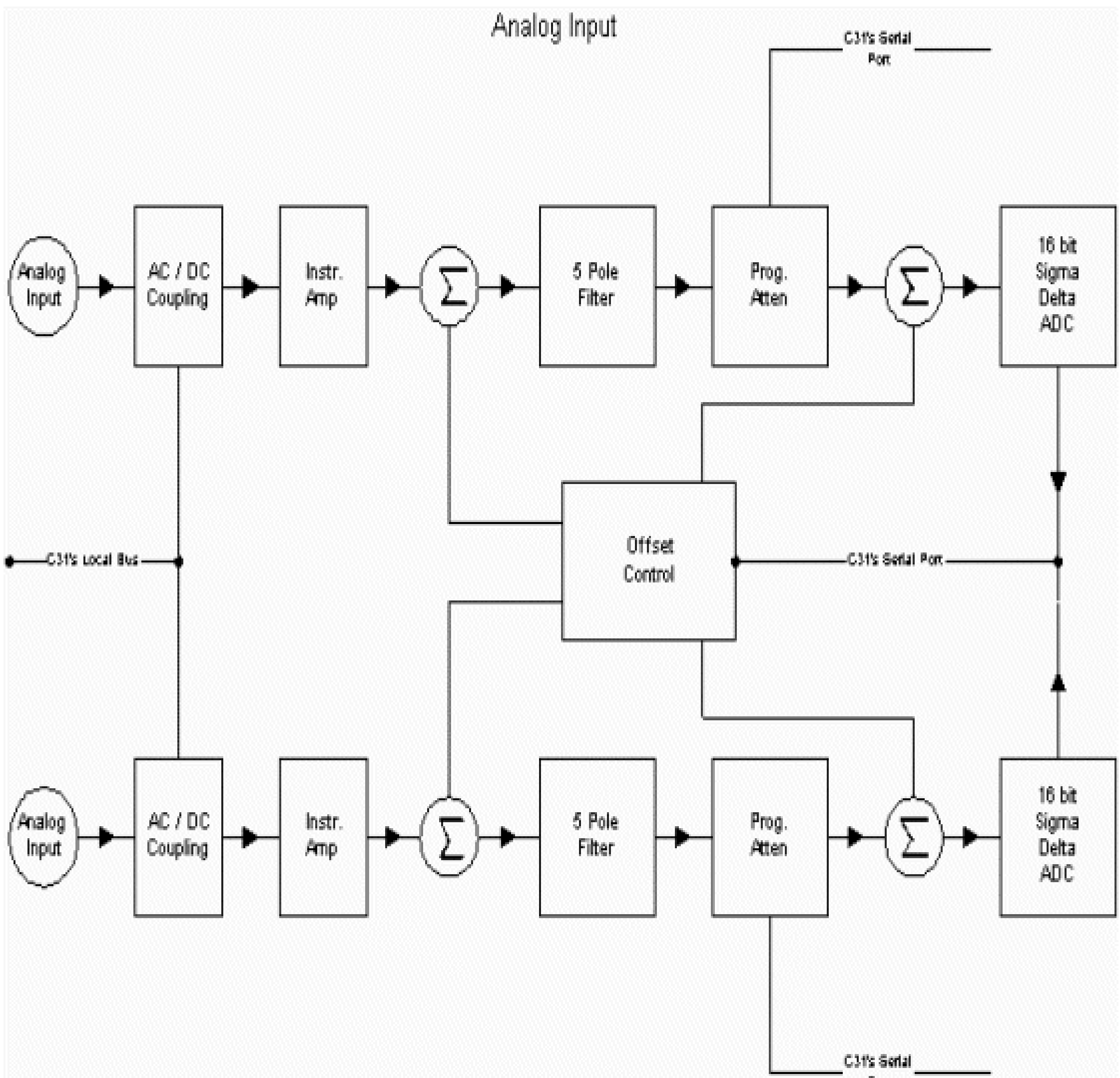

Figure 4. JAGUAR Input Daughter Card

The Mdsp3 board supports commercially available PCI Mezzanine SCSI disk controllers. The VxWorks RTOS can also be configured to support SCSI throughput disk (TPD) drives. The Spectral Dynamics' acquisition I/O driver allows applications to write all of the ADC data directly to the TPD drives in each ACP. Replay and data conversion features are available from selected software applications listed later in this paper.

Software Design Concepts

The basic software architecture for the workstation was originally designed for the previous generation of Spectral Dynamics control and analysis systems. The design has been extended as needed to take advantage of new hardware features, commercial OS features and other industry standards. The general graphical user interface (GUI) features are nearly identical to earlier implementations so that the need for additional training is minimal.

The lower-level software that runs in each ACP is key to the success of the overall product, especially for high bandwidth, high performance, high channel count applications. An overview of the Mdsp3 software is shown in Figure 5. The Mdsp3 processor is programmable in high-level computer languages, such as "C". The section labeled "MDSP Code" is downloaded from the host disk drive for each application. It could be the entire control loop for the Swept Sine application or relatively simple triggering code for a signal analyzer program.

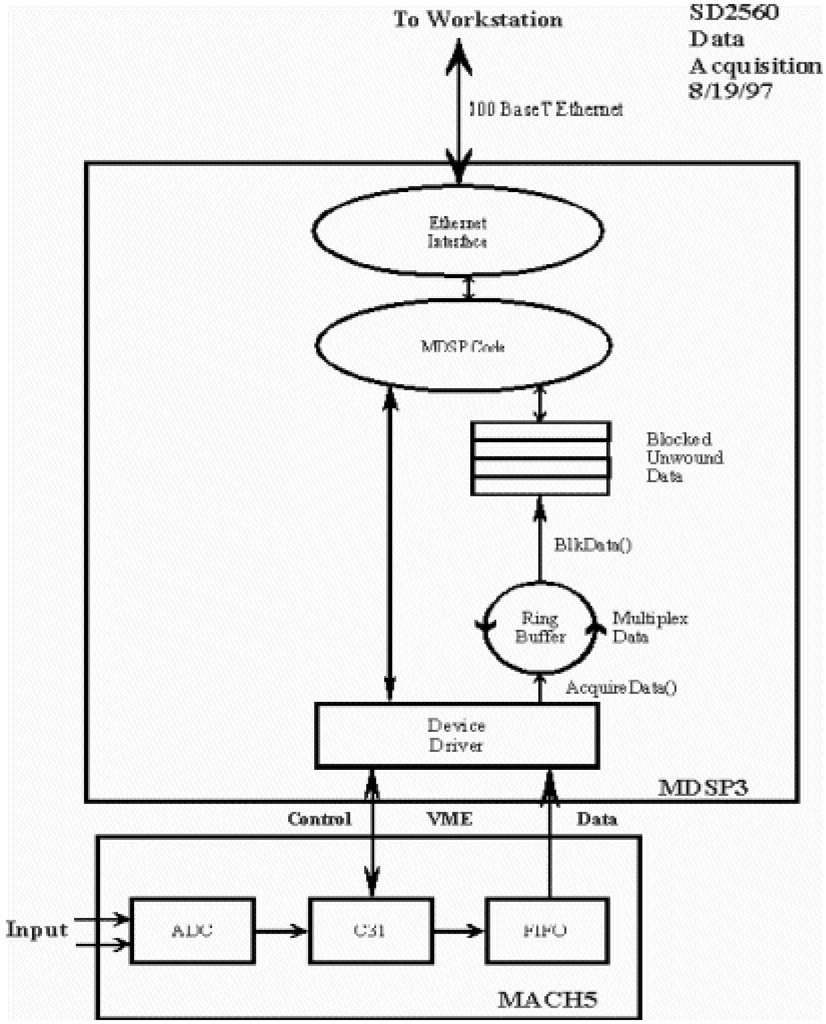

Figure 5. MDSP3 Software Overview

The acquisition I/O device driver implements most of the specialized functions required by the various control system and signal analyzer applications. The data buffering is handled by a ring buffer scheme in conjunction with hardware FIFOs in order to achieve the highest possible performance. This algorithm takes advantage of peak burst rates available from the various processors, buses and interfaces. The ring buffer and FIFO are essentially allowed to "get behind" for awhile, as long as they "catch up" again on the average. The ring buffer implementation is further illustrated in Figures 6 and 7.

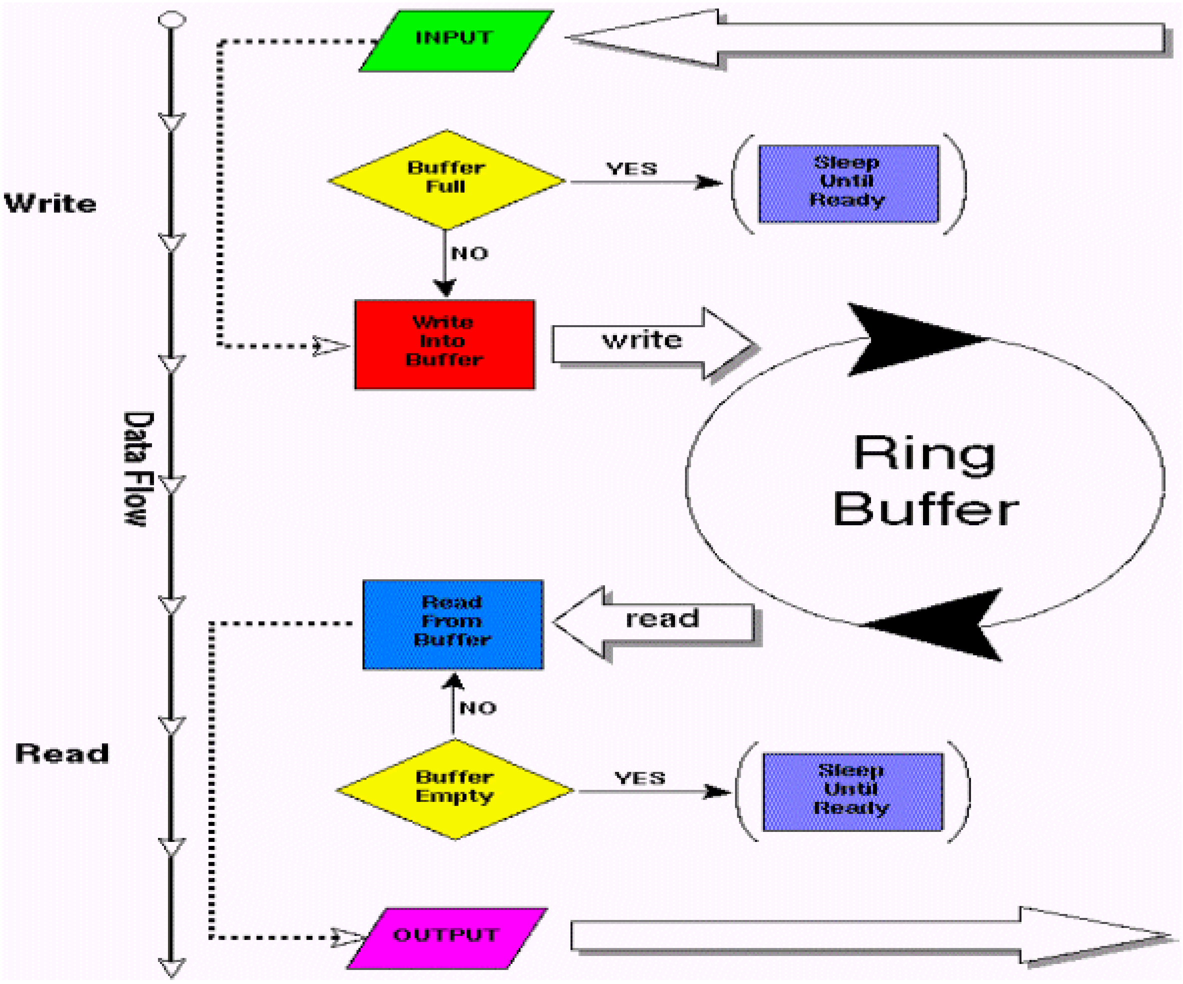

Figure 6. Acquisition Driver Ring Buffer

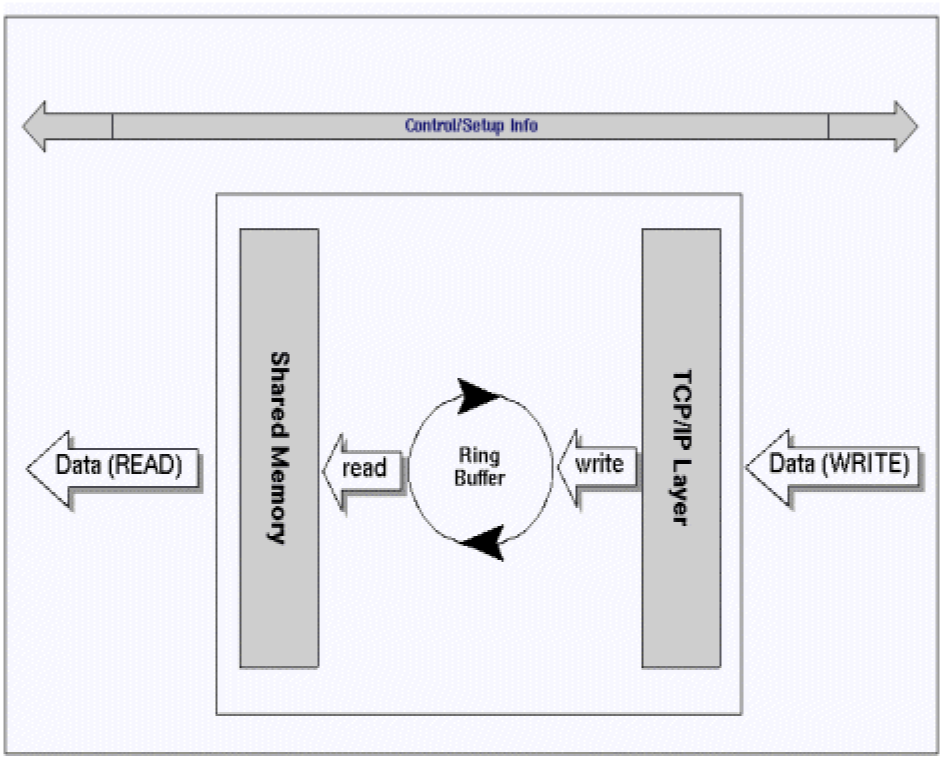

Figure 7. Acquisition Ring Buffer Network Layer

Turn-Key Applications

Spectral Dynamics has a long history and proven record for supplying turn-key solutions for data acquisition and control system applications. The original products date back to the 1960's and 1970's with the product lines produced by the original Spectral Dynamics and by Time Data/Genrad. Additional mergers have allowed incorporation of technology from the former SMS, STI and DSP Technology (via MTS) product lines. The following applications are currently fully supported on the system described in this paper:

- Single Exciter Control
  - Random Shaker Control & Analysis
  - Swept Sine Shaker Control & Analysis
  - Mixed-Mode Shaker Control & Analysis
  - Classical Shock Control & Analysis
  - Shock Synthesis (SRS) Control & Analysis
  - Waveform Replication Control
- Environmental Lab Signal Analysis & Synthesis
  - Shock Transient Capture & Analysis
  - General Purpose Signal Analyzer, Output Generator & Data Reviewer
  - Swept Sine Analysis
  - STAR Modal
  - Data Conversion Utility
  - Waveform Processor Utility
  - Seismic Synthesis Utility
- Multiple Exciter Control
  - MIMO Random Shaker Control

    - MIMO Swept Sine Shaker Control
    - MIMO Shock Control & Analysis
    - MIMO Waveform Replication
- Shared Parameters & System Support
    - Throughput Disks (Up to 6 for each ACP)
    - System Parameters Utilities
        - Remote Communication
        - Shaker Limits
        - System Channel Table
        - Import Sensor Table (spreadsheet)
        - Remote Control Panel
        - Mission Profile
    - ACP Diagnostics & Calibration (with full GUI & documentation for customer operation)
- Third-Party Applications with Direct Support
    - I-DEAS from MTS
    - Oasis Signal Conditioning (import sensor table) from Endevco
    - DynaWorks from Intespace.
    - Matlab from The MathWorks Inc.
    - StarOffice from Sun
    - SunForum from Sun & NetMeeting from Microsoft!

All of these applications run on the same single system! No other system in the world can come close to matching this list of applications. The Jaguar system can be configured with as few as 8 input channels and 1 output channel. It can grow into a system with up to 588 synchronized input channels.

A 508 channel system is fully operational for production satellite testing at NASDA in Japan. The same facility uses a Jaguar Multiple Exciter Control System with 66 input channels for control and limit/notching and 4 drive channels to control one table with 4 vertical exciters and another slip-table with 1 horizontal exciter.

The operating details for the listed applications are not in the scope of this paper. Separate technical papers, data sheets and/or operating manuals are available for each of the applications.

Host Workstations

The Jaguar Systems currently use a family of high performance RISC-based desktop workstations manufactured by Sun Microsystems. The Jaguar inherits all of the advances in hardware technology and OS technology provided by Sun.

The description for the base Sun Blade 100 includes:

- 500 MHz CPU with 256 KB L2 Cache
- 128 MB RAM Memory
- 15 GB 7200 RPM Disk
- CD-ROM Drive & 3.5" Floppy Drive
- 2 Ethernet ports (1 used for ACP)
- 1 serial port (used for ACP terminal window)
- 1 parallel port (for optional printer)

- 4 USB ports (2 used for keyboard/mouse)
- 2 IEEE 1394 ports
- Smart Card Reader
- Solaris 8 OS (or newer)

This workstation may be selected for configurations that include up to 38 input channels and a maximum of 1 Drive channel. Additional memory is added for higher channel counts.

The higher-end Blade 1000 or 2000 are recommended when the channel count requires 4 or more ACPs. These workstations includes:

- 750-1024 MHz CPU with 8MB Cache
- 1-8 GB RAM Memory
- 36-72 GB 10000 RPM FC-AL Disk
- PGX64 Graphics
- DVD-ROM Drive & 3.5" Floppy Drive
- 2 Ethernet ports (1 used for lab network, 1 used for 1st ACP)
- 2 serial ports (1 used for 1st ACP terminal window)
- 1 parallel port (for optional printer)
- 4 USB ports (2 used for keyboard / mouse)
- 2 IEEE 1394 ports
- Smart Card Reader
- Solaris 8 OS (or newer)

This workstation may be selected for configurations that include up to 392 input channels and a maximum of 8 Drive channels (within 4 ACPs). Additional Ethernet ports are required (an additional single port for up to 2 ACPs or the quad-port for up to 4 ACPs) and the serial port expansion option is required when more than 2 serial ports are needed.

For configurations with 5 or 6 ACPs, a 2nd CPU with 8MB Cache is added to the Blade 1000/2000 workstation. Additional RAM is also added to bring the total up to 2 GB (typical). The workstation can support up to 8 GB of RAM. No application or OS software changes are required. The same applications software that runs in an eight channel system also runs in a 588 channel system with a dual CPU workstation!

References

- Jaguar System Requirements & Design Documents (1997-2002). Not available for publication.
- Jaguar System Description Manual, part number 2560-0100/B, January 2001.
- Jaguar Service Manual, part number 2560-0101/A, January 1999.

Author's Biography

Kenneth Bosin is the Engineering Manager for Jaguar Systems at Spectral Dynamics in San Jose, CA. He has a BSEE from the University of Wisconsin and a MSEE from San Jose State University. His early experience was in defense, aerospace and automotive systems engineering and digital signal processing applications. He later joined the Time Data /

Genrad organization that was eventually merged into the "new" Spectral Dynamics. He now has over 25 years of experience in all phases of the design, development, integration and support of high performance data acquisition and control systems used primarily for environmental testing (shock and vibration) applications.